Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4139	257/314-316,321,324.ccls.	US-PGPUB; USPAT	OR	ON	2005/10/26 07:56
L2	2842	1 and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/10/26 07:56
L3	1297	2 and (bit adj line)	US-PGPUB; USPAT	OR	ON	2005/10/26 07:57
L4	1105	3 and (word adj line)	US-PGPUB; USPAT	OR	ON	2005/10/26 07:55
L5	949	438/261-263.ccls.	US-PGPUB; USPAT	OR	ON	2005/10/26 07:56
L6	678	5 and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/10/26 08:11
L7	614	6 not 4	US-PGPUB; USPAT	OR	ON	2005/10/26 07:57
L8	250	7 and (bit adj line)	US-PGPUB; USPAT	OR	ON	2005/10/26 08:09
L9	367	((word adj line) and (bit adj line) and memory and plurality and (dielectric or insulating or insulator or insulative) and nitride and oxide).clm.	US-PGPUB; USPAT	OR	ON	2005/10/26 08:11

DOCUMENT-IDENTIFIER: US 20020151138 A1

TITLE: Method for fabricating an NROM

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Abstract Paragraph - ABTX (1):

Nitride read only memory (NROM) fabrication begins with a substrate with a surface of the substrate having at least one memory area and one peripheral area. An oxide-nitride-oxide (ONO) layer, containing a bottom oxide layer, a silicon nitride layer and a top oxide layer, is formed to cover both the memory area and the periphery area. Multiple columns of **bit line** masks are then located on the ONO layer of the memory area. Numerous ion implantation and etching processes are performed on the substrate to finally form multiple rows of word lines, being approximately perpendicular to the **bit lines,** on the ONO layer.

Summary of Invention Paragraph - BSTX (6):

[0005] Please refer to FIG. 1 to FIG. 6. of cross-sectional views of forming an NROM cell according to the prior art. As shown in FIG. 1, an NROM cell is formed on the surface of a P-type silicon substrate 10. The prior art method first performs an ONO process on the surface of the P-type silicon substrate 10 to form an ONO dielectric layer 18 composed of a bottom oxide layer 12, a silicon nitride layer 14 and a top oxide layer 16. A photolithographic process is employed to form a photoresist layer 20 on the surface of the ONO dielectric layer 18. The photoresist layer 20 forms patterns to define positions of **bit lines**.

Summary of Invention Paragraph - BSTX (7):

[0006] As shown in FIG. 2, the photoresist layer 20 is used as a mask for performing an anisotropic etching process to remove the top oxide layer 16 and the silicon nitride layer 14 not covered by the photoresist layer 20. Following that, an ion implantation process 22 is performed to form a plurality of N-type doped areas 24 in the silicon substrate 10 that function as **bit lines,** i.e. buried drains of the memory device. Two neighboring doped areas 24 define a channel, and the distance between the two neighboring doped areas 24 is defined as channel length. The ion implantation process 22 is performed perpendicular to the surface of the silicon substrate 10 using an arsenic (As) ion concentration of 1.times.10.sup.14.about.1.times.10.sup.16/cm.sup.2 and having an energy ranging from 20 KeV to 200 KeV at room temperature.

Summary of Invention Paragraph - BSTX (11):

[0010] As shown in FIG. 6, a thermal oxidation method with a temperature of 700.degree. C..about.1150.degree. C. is employed to form a **bit line** oxide layer 32 on a top surface of the **bit lines** 24 so as to separate each silicon nitride layer 14. Finally, a doped polysilicon layer 34 is deposited and functions as a word line. The dopants implanted into the silicon substrate 10 previously, including the dopants in the doped areas 24, 28 and 29, can be activated during the formation of the **bit line** oxide layer 32.

Summary of Invention Paragraph - BSTX (12):

[0011] However, two ion implantation processes, having a first oblique angle 26 and a second oblique angle 27, respectively, lead to several problems. Neither the doped areas 28 and 29 of p-type have a distributed depth of doped concentration at a short distance, less than 500 angstroms, away from the surface of the silicon substrate 10 so as to improve programming efficiency. In addition, the diffusion profile of the dopants is difficult to control due to the sloping concentration distribution of the dopants in the doped areas 28 and 29 after the **bit line** oxide layer 32 is formed by performing the thermal oxidation process. Besides, a complicated calculation is needed to precisely control the required concentration distribution, diffusion profile of the dopants, parameters of the ion implantation processes, including the first and second oblique angles 26 and 27, implantation energies and dosages. The production window is thus reduced. Consequently, the production cost is increased as well.

Summary of Invention Paragraph - BSTX (17):

[0015] According to the claimed invention, a substrate with a surface comprising at least one memory area and one peripheral area is provided in a method for fabricating a NROM. An oxide-nitride-oxide (ONO) layer, comprising a bottom oxide layer, a silicon nitride layer and a top oxide layer, is formed to cover both the memory area and the periphery area. Multiple columns of **bit line** masks are then formed on the ONO layer of the memory area. By performing a first ion implantation process of a first conductive type, a plurality of **bit lines** of the first conductive type is formed within the substrate not covered by the **bit line** masks. An etching process is then performed to etch the **bit line** masks to a predetermined depth. By performing a second ion implantation process of the second conductive type approximately perpendicular to the ONO layer, a plurality of ultra-shallow doped areas of the second conductive type is formed within the substrate not covered by the **bit line** masks. Finally, the **bit line** masks are removed and a plurality of rows of word lines, approximately perpendicular to the **bit lines,** is formed on the ONO layer at the end of the

method.

Summary of Invention Paragraph - BSTX (18):

[0016] It is an advantage of the present invention that after the etching process, the **bit line** masks still have enough thickness to function as implantation masks in the subsequent ion implantation process. In addition, the ultra-shallow doped areas, having a doped depth smaller than 500 angstroms and a bottom width of the doped channel of approximately 100 angstroms, are close to the surface of the substrate and helpful to produce hot carrier. Therefore, the programming efficiency of the NROM is significantly improved.

Detail Description Paragraph - DETX (2):

[0020] Please refer to FIG. 7 to FIG. 11 of the cross-sectional views of forming an NROM cell according to the present invention. As shown in FIG. 7, an oxide-nitride-oxide (ONO) process is performed to form an ONO layer 58, having a thickness ranging from 150 to 250 angstroms, on a surface of a silicon substrate 50, further comprising at least a memory area and a peripheral area. For simplicity of the description, only portions of the memory area relative to the present invention are revealed in FIG. 7 to FIG. 11. The ONO layer 58 further comprises a bottom oxide layer 52, having a thickness ranging from 50 to 150 angstroms, a silicon nitride layer 54, having a thickness ranging from 20 to 150 angstroms, and a top oxide layer 56, having a thickness ranging from 50 to 150 angstroms. A lithography process is then performed to form a photoresist layer 60, employed to define patterns of a buried drain or **bit lines,** on the ONO layer 58. In the preferred embodiment of the present invention, the silicon substrate is a P-type silicon substrate with the <100> bottom surface. The method of the present invention is applied not only to the P-type silicon substrate but also to others like the silicon-on-insulator (SOI) substrate, comprising a P-type silicon layer and an insulator layer (both not shown), made by a separation by implantation oxygen (SIMOX) process. The method of fabricating the SOI substrate, normally having a thickness ranging from 0.5 to 3 microns, is not the major element of the present invention and is omitted in the following discussion.

Detail Description Paragraph - DETX (4):

[0022] As shown in FIG. 8, an anisotropic dry etching process, using the photoresist layer 60 as a mask, is performed to remove portions of the top oxide layer 56 and portions of the silicon nitride layer 54, not covered by the photoresist layer 60. An ion implantation process 62 is then performed to form multiple doped areas 64 of n-type, employed as **bit lines** of the memory, in the silicon substrate 50. A channel is defined as a space between two neighboring doped areas 64 and a channel length is thus defined as the distance between two

neighboring doped areas 64. The dosage of the ion implantation process, using arsenic (As) ions as primary dopants to perpendicularly dope the silicon substrate 50 at a room temperature, is 1.times.10.sup.14 to 1.times.10.sup.16 cm.sup.-2 with an implantation energy ranging from 20 to 200 KeV. In another embodiment of the present invention, other n-type ions, including phosphorous (P) ions, are employed as the dopants of the ion implantation process.

Detail Description Paragraph - DETX (8):

[0026] As shown in FIG. 11, a thermal oxidation process with a operating temperature of 700.degree. C..about.1150.degree. C. is employed to form a **bit line** oxide layer 72 on a top surface of the **bit lines** 64 so as to separate each silicon nitride layer 54. Finally, a doped polysilicon layer 74 is deposited and functions as a word line. The dopants previously implanted into the silicon substrate 50, including the dopants in the doped areas 64 and 69, can be activated during the formation of the field oxide layer 72.

Claims Text - CLTX (2):

1. A method for fabricating a nitride read only memory (NROM), the method comprising: providing a substrate, with the surface of the substrate comprising at least one memory area and one peripheral area; forming an oxide-nitride-oxide (ONO) layer to cover both the memory area and the periphery area, the ONO layer comprising a bottom oxide layer, a silicon nitride layer and a top oxide layer; forming a plurality of columns of **bit line** masks on the ONO layer of the memory area; performing a first ion implantation process of the first conductive type to form a plurality of **bit lines** of the first conductive type within the substrate not covered by the **bit line** masks; etching the **bit line** masks to a predetermined depth, with the remaining **bit line** masks still having enough thickness to function as implantation masks in the subsequent ion implantation process; performing a second ion implantation process of the second conductive type approximately perpendicular to the ONO layer to form a plurality of ultra-shallow doped areas of the second conductive type within the substrate not covered by the **bit line** masks; removing the **bit line** masks; and forming a plurality of rows of word lines on the ONO layer, the word lines being approximately perpendicular to the **bit lines**; wherein the ultra-shallow doped areas being close to the surface of the substrate and helpful to produce hot carrier so as to improve the programming efficiency of the NROM.

Claims Text - CLTX (3):

2. The method of claim 1 wherein before forming the **bit line** masks the method further comprises: forming at least one mask on the ONO layer of the memory area; performing a second ion implantation process to adjust a dopant

concentration of the substrate not covered by the mask; and removing the mask.

Claims Text - CLTX (5):
4. The method of claim 1 wherein the **bit line** masks comprise photoresist materials.

Claims Text - CLTX (8):
7. The method of claim 1 wherein the plurality of ultra-shallow doped areas of second conductive type are next to the **bit lines**.